Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A variable delay line comprising:

a hybrid coupler [[(12)]] having an input terminal [[(22)]] for being supplied with an input signal, first and second output terminals [[(14, 16)]] for outputting first and second output signals, respectively, which are 90° out of phase with each other, and an isolation terminal [[(24)]] for outputting a reflected signal based on said first and second output signals as a third output signal; and

first and second reactance parts [[(18, 20)]] connected respectively to said first and second output terminals [[(14, 16)]] and having substantially same reactances;

wherein said first and second reactance parts [[(18, 20)]] have first and second variable-reactance devices, respectively, having substantially same reactances.

2. (Currently Amended) A variable delay line according to claim 1, wherein said first and second reactance parts [[(18, 20)]] comprise respective series-connected circuits of first and second capacitors [[(38, 40)]] having substantially same capacitances, first and second variable-capacitance devices [[(26, 42)]] as said first and second variable-reactance devices, and a first resonant circuit [[(30, 46)]] and a second resonant circuit [[(32, 48)]].

3. (Currently Amended) A variable delay line according to claim 2, wherein series-connected circuits of third and fourth capacitors [[(54, 56)]] and third and fourth variable-capacitance devices [[(58, 60)]] as variable-reactance devices are connected in parallel to said first resonant circuit [[(30, 46)]] and said second resonant circuit [[(32, 48)]].

4. (Currently Amended) A variable delay line according to claim 2[[or 3]], wherein a plurality of ceramic layers are stacked to form an integral structural body[[(78)]], said integral structural body [[(78)]] having a ceramic layer [[(66)]] with said hybrid coupler [[(12)]] disposed thereon, a ceramic layer [[(68)]] with said first resonant circuit [[(30, 46)]] and said second

resonant circuit [[(32, 48)]] disposed thereon, and a ceramic layer [[(70)]] with at least said first and second capacitors [[(38, 40)]] disposed thereon.